ABSTRACT OF THE DISCLOSURE

A gate process and a gate process for an embedded memory device. A semiconductor silicon substrate has a memory cell area and a logic circuit area. A first dielectric layer is formed overlying the semiconductor silicon substrate, and then a gate structure is formed overlying the first dielectric layer of the memory cell area. Next, a protective layer is formed overlying the first dielectric layer and the top and sidewall of the gate structure. Next, an insulating spacer is formed overlying the protective layer disposed overlying the sidewall of the gate structure. Next, a pre-cleaning process is performed to remove the protective layer and the first dielectric layer overlying the logic circuit area. Next, a second dielectric layer is formed overlying the logic circuit area, and then a gate layer is formed overlying the second dielectric layer of the logic circuit area.